The input data bits of the illustrative embodiment can be represented by a matrix such as shown in figure 6, in which each row represents a rail and each column represents a time slot. Each incoming STS-1 signal's data bit may be placed by a rail number and a slot number. Such a matrix will be referred to hereinafter as an input bit map. Similarly, the switches output may be represented by an output bit map in which each outgoing STS-1 channel is identified by an outgoing rail number and time slot number. A physical embodiment for the input and output bit maps may be realized by employing a selection block, 701, as in Fig. 7, for each of the seven hundred and sixty eight input or output data bits of the illustrative embodiment.

REMARKS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application and that claims 1-22 stand rejected. By this response, all claims continue un-amended.

In view of both the amendments presented above and the following discussion, the Applicants submit that none of the claims now pending in the application is anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Furthermore, the Applicants also submit that these claims now satisfy the requirements of 35 U.S.C. § 112. Thus, the applicants believe that all of the claims are now in allowable form.

Rejections

A. 35 U.S.C. § 112

The Examiner has rejected claims 1-22 under the provisions of the first paragraph of 35 U.S.C. § 112 as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Specifically, the Examiner alleges that "Claims 1, 5, 6, 11, 16, and 20 use the term 'time slot.' The specification fails to define 'time slot' as it relates to the claimed invention."

It is respectfully submitted that both the significance and meaning of the term "time slot" is clear to those skilled in the relevant art. Within the context of a switching architecture such as disclosed by the inventors, the use of the term "time slot" is consistent throughout the disclosure and consistent with the common meaning of the term. As is well known to those skilled in the art, the concept of "slotting" is used to divide existing bandwidth into a plurality of slots, such as time slots, frequency slots and the like. That is, given an available bandwidth, the use of that bandwidth is allocated among a plurality of channels by temporally dividing the bandwidth among the channels.

Within the context of the switch architecture of the present invention, a "time slot" is sized to accommodate bit packs of the desired size and at the desired data rate. The tradeoffs between space and time switching are noted in the paragraph bridging pages 9 and 10, and the embodiments that follow. For example, in the embodiment of Figure 4 (discussed beginning on page 10, line 3), a 4:2 multiplexer 402 routes data from two inputs (C1B1 and C2B2) during a first time slot, and data from the remaining two inputs (C3B1 and C4B1) during a second time slot. The time slots are defined by the number of bits switched within a single time slot and the data rate of those bits to be switched.

The Examiner further alleges that "the apparatus and its method of use, as described in claims 1, 5, 6, 11, 16, and 20, is sufficiently complex that a reasonably detailed description, including a set of detailed drawings, is necessary to enable one of ordinary skill in the art to make or use the invention as claimed." Furthermore the Examiner refers to Van Hoogenbemt (U.S. Patent 6,169,736 issued Jan. 2, 2001) stating that "According to Van Hoogenbemt, the selector circuitry is very complex (column1, lines 21-25; column 1, lines 35-40)".

The Examiner seems to assert that the naked characterization of a functional element, apparatus or method as "complex" by the author of a cited

reference should somehow set the standard for an enabling disclosure in the present patent application. The Applicants strongly disagree with this assertion. First, whether something is "complex" or "non-complex," the relevant inquiry is whether one skilled in the art can practice the subject invention without undue experimentation. It is respectfully submitted that those skilled in the very sophisticated art of creating switch fabrics or switch architectures are more than able to practice the claimed invention given the instant disclosure. That the author of the Van Hoogenbemt patent deemed something to be "complex" has no bearing on whether the disclosure of the present patent application enables one skilled in the art to practice the claimed invention. The Applicants agree that the subject matter of the claimed invention is a non-trivial technology.

Therefore, the Applicants submit that claims 1, 5, 6, 11, 16, and 20 as they now stand, fully satisfy the requirements of 35 U.S.C. § 112 and are patentable thereunder.

Furthermore claims 2-4, 7-10, 12-15, 17-19, 21, and 22 depend, either directly or indirectly from claims 1, 5, 6, 11, 16, and 20 and recite additional features therefor. As such and for the exact same reasons set forth above, the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 112 and are patentable thereunder.

In view of changes made to the specification and the above discussion, the Applicants submit that claims 1-22, as they now stand, do not contain any subject matter not described in the specification and do enable one skilled in the art to which it pertains to make and/or use the invention, and hence fully satisfy the requirements of 35 U.S.C. § 112.

B. 35 U.S.C. § 102

The Examiner rejected claims 1-5 under 35 U.S.C. 102(b) as being anticipated by Tocci, Digital Systems: Principles and Applications, 3rd edition (Prentice Hall, Inc. 1985, Pages 388-394). The rejection is respectfully traversed.

Tocci discloses a demultiplexer for switching a single input and distributing it over several outputs. (See Tocci, page 388). Tocci falls, though, to disclose at least the invention as recited in Applicants' claim 1 as follows:

> "Apparatus for switching data from any of a plurality of inputs to any of a plurality of outputs, comprising:
> apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots,
> apparatus for selecting one of the input bit packs from one of the rails in one of the time slots, and
> apparatus for conveying said selected bit pack to an output data position within a combination of output data rails and time slots." (emphasis added)

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrik Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)) (emphasis added).

In contrast to the above quoted claim language, Tocci merely teaches an apparatus such that a single input data line is connected to all of the output gates, wherein the output gates will be enabled by select codes, routing the data to the appropriate output lines. (See Tocci, page 388-389). Subsequently, the apparatus disclosed in Tocci is incapable of switching data from "any of a plurality of inputs to any of a plurality of outputs".

Therefore, the Applicants submit that claim 1 is not anticipated by the teachings of Tocci and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 5 recites similar features as recited in claim 1. As such, the Applicants submit that independent claim 5 is not anticipated by the teachings of Tocci and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 2-4, depend either directly or indirectly from claim 1 and recite additional features therefor. As such and for the exact

same reasons set forth above, the applicants submit that none of these claims is anticipated by the teachings of Tocci. Therefore the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

C. 35 U.S.C. § 103(a)

The Examiner has rejected claims 6,11, and 16-22 under 35 U.S.C. § 103(a) as being unpatentable over the Van Hoogenbemt patent (United States patent 6,169,736 issued Jan. 2, 2001). The rejection is respectfully traversed.

The Examiner conceded in paragraph 7 of the Office Action that "Van Hoogenbemt does not explicitly state the number of time slots or the number of input or output rails." However, the Examiner alleges that "the interfacing device inherently uses some number, T, time slots for the input; some number, T2, of time slots for the output; some number, R, of input rails; and some number, R2 of output rails." As such the Examiner concluded that "it would have been obvious to one of ordinary skill in the art to modify the invention of Van Hoogenbemt so that the number of inputs to each multiplexer is the same as the number of input rails because through appropriate modification of the selection inputs to the multiplexers any combination of inputs could be output from the set of multiplexers, and any change in strategy could easily be implemented through modification of software that controls the selection inputs." Applicants respectfully disagree.

Applicants have defined an apparatus for switching data from any input position to any output position. Specifically, Applicants' claim 6 positively recites:

> "Apparatus for switching data from any of N input positions arranged as T time slots on R rails to any of M output positions arranged as T2 time slots on R2 rails, comprising:
> M selection blocks, each configured to select a bit pack for a different one o f the output positions, and each including:
> apparatus for receiving input data arranged as bit packs in T time slots on R rails,

apparatus for selecting data from one of the R ralls and latching the selected data during a predetermined time slot to thereby select a bit pack of predetermined R and T values, and

apparatus for conveying said selected bit pack to an output position of predetermined T2 and R2 values." (emphasis added)

In contrast to the above quoted claim, Van Hoogenbemt teaches an interfacing device that can only arrange the output data with respect to the order in which the input data is selected. "The outgoing nibbles are applied to the outgoing channel OC in the order of the memory cells OS1, OS2, ..., OSM wherein they are stored. Since the interfacing device INT outputs nibbles in the order wherein they arrive, a nibble stored in a lower memory cell of the incoming register IR also has to be stored in a lower memory cell of the outgoing register OR." (emphasis added) (See Van Hoogenbemt, column 6, lines 48-55). Furthermore, Van Hoogenbemt teaches that to achieve any other particular order in the outgoing sets of bits, physical connections have to be altered. "Evidently, any other particular order in the outgoing sets of bits can be realized by selecting the distinct N-M+1 incoming sets of bits that are applied to MUX1, MUX2, . . ., MUXM respectively in an appropriate way and by interconnecting the logical cells constituting the matrix in CTRL also in an appropriate way." (See Van Hoogenbemt, column 9, lines 22-27). Therefore, it is impossible for the interfacing device in Van Hoogenbemt to be used "for switching data from any of N input positions" "to any of M output positions", and furthermore, it would not be obvious to one of ordinary skill in the art to modify the invention of Van Hoogenbemt to do so in the manner of Applicants' present invention.

As such, the Applicants respectfully submit that Van Hoogenbemt does not teach or suggests or make obvious Applicants' claim 6. Therefore, the Applicants submit that claim 6 fully satisfies the requirements of 35 U.S.C § 103 and is patentable thereunder.

Likewise, independent claims 11, 16 and 20 recite similar features as recited in claim 6. As such, the Applicants submit that independent claims 11, 16

and 22 are not obvious under the teachings of Van Hoogenbemt and also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Furthermore, dependent claims 17-19, and 21-22, depend either directly or indirectly from claims 16, and 20 and recite additional features therefor. As such and for the exact same reasons set forth above, the applicants submit that none of these claims are obvious under the teachings of Van Hoogenbemt. Therefore the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Conclusion

Thus the Applicants' submit that none of the claims, presently in the application, is anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. §103. Furthermore, the Applicants also submit that all of these claims now fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

E J Wall

Eamon J. Wall Attorney
Reg. No. 39,414

Dated: 1/29/02

CUSTOMER #26,291
MOSER, PATTERSON & SHERIDAN, LLP
595 Shrewsbury Avenue, Suite 100
Shrewsbury, New Jersey 07702
732-530-9404 - Telephone
732-530-9808 – Facsimile

MARKED UP SPECIFICATION

At page 11, beginning with line 22 and ending with line 27, please replace the paragraph beginning " The input data bits..." and ending "...time slot number." with:

> The input data bits of the illustrative embodiment can be represented by a matrix such as shown in figure 6, in which each row represents a rail and each column represents a time slot. Each incoming STS-1 signal's data bit may be placed by a rail number and a slot number. Such a matrix will be referred to hereinafter as an input bit map. Similarly, the switches output may be represented by an output bit map in which each outgoing STS-1 channel is identified by an outgoing rail number and time slot number. A physical embodiment for the input and output bit maps may be realized by employing a selection block, 701, as in Fig. 7, for each of the seven hundred and sixty eight input or output data bits of the illustrative embodiment.